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New claims

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1. Phase/frequency-locked loop (1) having a phase/frequency comparator (8) and a frequency-generating oscillator (10), the phase/frequency comparator (8) having two edge-triggered storage devices (13, 14) which are
10 respectively set by an edge of a reference-frequency signal (4), whose frequency may be divided if required, for the phase/frequency locked loop (1), and by an edge of an output-frequency signal (6), whose frequency may be divided if required, from the phase/frequency locked loop (1), and
15 which are each reset by an output signal (16) from a resetting logic unit (15) to whose inputs are supplied the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14), characterised in that the output signal (16) from the resetting logic unit (15) is only activated
20 when both the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14) have been activated, and is only de-activated when both the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14) have been deactivated, and in that the resetting logic unit (15)
25 is implemented by means of an asynchronous level-triggered RS storage device (17) of inverse logic, the resetting input of the asynchronous level-triggered RS storage device (17) having the output signal (20) from an OR gate (21) supplied to it, and in that the two edge-triggered storage
30 devices (13, 14) each have only an output of non-inverted logic.

2. Phase/frequency-locked loop according to 1, characterised in that the output (Q) of the edge-triggered storage device (13), to whose input (Clk) the reference-frequency signal (3), whose frequency may be divided if required, is applied is fed to the frequency-generating oscillator (10) to increase the frequency of the output-frequency signal (6), and the output (Q) of the edge-triggered storage device (14), to whose input (Clk) the output-frequency signal (6), whose frequency may be divided if required, is applied is fed to the frequency-generating oscillator (10) to reduce the frequency of the output-frequency signal (6).

3. Phase/frequency-locked loop according to claim 1 and 2, characterised in that the signals (9A, 9B) at the outputs (Q) of the two edge-triggered storage devices (13, 14) are connected to the frequency-generating oscillator (10) via an interposed loop filter (11) for stabilising the phase-frequency-locked loop (1).

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4. Phase/frequency-locked loop according to one of claims 1 to 3, characterised in that the frequency of the reference-frequency signal (2) to the phase/frequency-locked loop (1) is reduced by a factor N by means of a frequency divider (2), upstream of the input (Clk) of the phase/frequency comparator (8).

5. Phase/frequency-locked loop according to one of claims 1 to 4, characterised in that the frequency of the output-frequency signal (6) from the phase/frequency-locked loop (1) is reduced by a factor M by means of a frequency divider (5), upstream of the input (Clk) of the phase/frequency comparator (8).

6. Phase/frequency comparator (8) for a phase/frequency-locked loop (1), having two edge-triggered storage devices (13, 14) which are respectively set by an edge of a reference-frequency signal (3), which may be divided if required, for the phase/frequency-locked loop (1), and by an edge of an output-frequency signal (6), which may be divided if required, from the phase/frequency-locked loop (1), and which are each reset by an output signal (16) from a resetting logic unit (15) to whose inputs are supplied the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14), characterised in that the output signal (16) from the resetting logic unit (15) is only activated when both the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14) have been activated, and is only de-activated when both the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14) have been de-activated, and in that the resetting logic unit (15) is implemented by means of an asynchronous level-triggered RS storage device (17) of inverse logic, the resetting input of the asynchronous level-triggered RS storage device (17) having the output signal (20) from an OR gate (21) supplied to it, and in that the two edge-triggered storage devices (13, 14) each have only an output of non-inverted logic.